**EE 2000 Logic Circuit Design Semester B 2022/23**

Tutorial 5

1. What are the mistakes for this VHDL?

**Library** ieEe;

**use** IEEE.std-logic\_1164.all;

ENTITY and\_gate IS

port (a&b : in STD\_LOGIC; S: out STD\_LOGIC;);

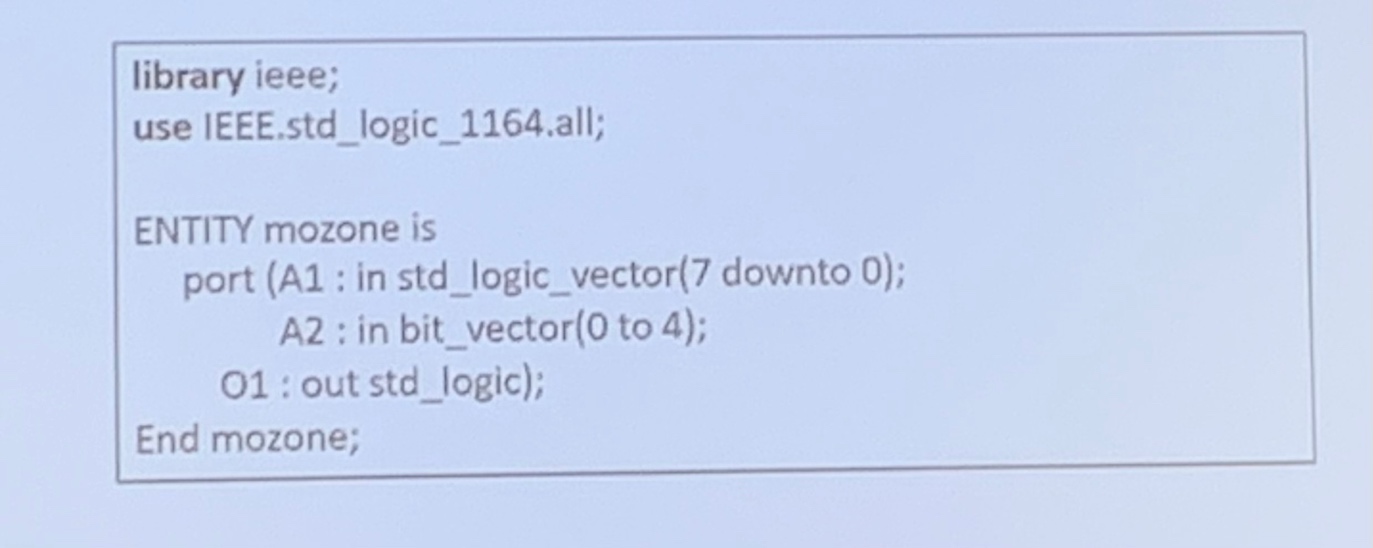
end;

architecture CKT of anD\_Gate IS begin

s <= a AND b;

end ckt;

1. Using VHDL to write the library and entity declarations for a logic design entity named MoZone that has the following inputs and outputs.
   1. A1 is an array of 8-bit std\_logic data with the highest index number holding the most significant bit.
   2. A2 is a 5-bit bit vector with the lowest index number holding the most significant bit
   3. O1 is a 1-bit std\_logic output



1. Write a complete VHDL design module (with entity and architecture) to implement a circuit with the following Boolean expressions. Use concurrent statements and without NAND and NOR operators in your design.

* x1 = A’B’C + A(BC)’
* x2 = (A’B + C’)(BC’ + A)’
* x3 = (A(BC)’ + A’C’)’

Graphical user interface, text, application, chat or text message

Description automatically generated

1. Write a complete VHDL design module to implement a circuit with the following Boolean expressions. Assign a signal name sigW1 to represent the common logic term in your design. Use concurrent statements without NAND and NOR operators in your design.

* A = (XY’Z’)’ + XZ
* B = (XY’Z’)’(X + Z)
* C = ((XY’Z’)’+X’)’

1. Write a complete VHDL design module to implement the combinational circuit shown. Assign signals for intermediate outputs. Use concurrent statements (i) without NAND and NOR operators in your design; and (ii) with NAND and NOR operators.

